Pixel Detector R&D

towards an ILC

Vertex Detector

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DESY/F1
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This Talk

- Introduction: ILC
- VXG considerations
- Sensor R&D
  - CCD, MAPS, DEPFET, …
- R&D Infrastructure: EUDET
- Conclusions
The ILC
(The next great project in HEPP)

- $E_{cm}$ adjustable from 200 – 500 GeV
- Luminosity $\Rightarrow \int L dt = 500 \text{ fb}^{-1}$ in 4 years
- Ability to scan between 200 and 500 GeV
- Energy stability and precision below 0.1%
- Electron polarization of at least 80%
- The machine must be up-gradeable to 1 TeV
Physics Motivation, e. g. Higgs

Determination of mass and width of the Higgs:
most favorable (light Higgs) \text{ee} \rightarrow \text{Z} \rightarrow \text{ZH}

\begin{align*}
\text{ZH} \rightarrow \mu \mu X & \quad \text{ZH} \rightarrow qqbb & \quad \text{ZH} \rightarrow WW qq
\end{align*}

Clear signals in many channels:

<table>
<thead>
<tr>
<th>mass \ Higgs</th>
<th>\Delta M</th>
<th>width:</th>
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<tbody>
<tr>
<td>120 GeV</td>
<td>40 MeV</td>
<td>5-10%</td>
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<tr>
<td>150 GeV</td>
<td>70 MeV</td>
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<td>180 GeV</td>
<td>90 MeV</td>
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Tracking/Vertexing

Need excellent reconstruction of secondary vertices

Higgs recoil Signal for changing tracker resolutions

\[ \sigma(1/p) = 7 \times 10^{-5} \text{GeV} \]

\[ \sigma(1/p) = 3 \times 10^{-4} \text{GeV} \]

Need precise measurement of the momenta of tracks

Improve the tracker precision by an order of magnitude

Couplings to fermions:
R&D for Tracking/Vertexing

Vertex Detector:
- multi layer, high precision pixel detector is required

Different technologies are being investigated:
CCD, MAPS, DEPFET, plus derivates

precision: μm level
material budget/ cooling / mechanics are main concerns
readout speed (minimise number of overlapping bunches)
General Considerations

- Impact parameter: \( \sigma_{ip} = 5 \mu m \oplus 10 \mu m/ \rho \sin^{3/2} \theta \)
- Minimal material: \( \leq 0.1\% X_0 \)
- Fast readout
- Radiation hard

1 train = \( \sim 3000 \) bunches in \( \sim 1 \) ms, 5Hz repetition rate
- Occupancy is too high to integrate over one train

- Readout
  - \( \sim 20 \times \) during train (every 50 \( \mu s \))
  - Between trains (store info in sensors)
  - Decrease pixel size + time stamping
Radiation and Backgrounds

- Operation at high background rates:
  0.04 hits/mm$^2$/BX in the inner layer (1.5 cm)
  - Occupancy of ~10% per bunchtrain
  - 20 frames per train (1 ms)
  - 40 MHz line rate => ½% Occup. (4096 lines along a 10 cm module)

- Radiation Hard up to 360 kRad
- and $10^{12}$ n/cm$^2$ (10 years)
Technology Options

- Readout every 50 μs:
  - CCDs, MAPS, DEPFET, SOI

- In-pixel memory and R/O between trains:
  - ISIS, FAPS

- Finer pixels and R/O between trains:
  - FPCCD (no bunch id)
  - Chronopixels (with bunch id)
CCDs and CPCCCDs

- CCD technology proven at SLD, but ILC sensors must be faster, more rad-hard
- Readout in parallel addresses speed concerns
- CPCCCD’s feature small pixels, can be thinned, large area, and are fast
- CPC1: two-phase, 400 (V) x 750 (H) pixels, each 20 $\mu$m2

"Classic CCD" Readout time $\approx N \times M / F_{out}$

Column Parallel CCD
Readout time = $N / F_{out}$
Column-Parallel CCDs

- First-generation tests (CPC1):
  - Noise ~100 e⁻ (60 e⁻ after filter).
  - Minimum clock potential ~1.9 V.
  - Max clock frequency above 25 MHz (design 1 MHz).
  - Limitation caused by clock skew

- Next generation now available (CPC2):
  - Busline free design (two-level metal)
  - Large area ‘stitched’ sensor, choice of epi layers for varying depletion depth
  - Range of device sizes for test of clock propagation (up to 50 MHz)
  - Large chips are nearly the right size

Raw ADC data at 1 MHz
\( \sigma_{\text{total}} = 3.92 \text{ ADC channels (62 electrons)} \)

ADC channel

CPC2-70
9.2 cm
CPC2: Next generation CCD

- CPC2: second generation Column-parallel CCD
  - Single-metal: (100 Ωcm @ 25 µm and 1.5 kΩcm @ 50 µm)
  - 2 more wafers received with 2-level metal (busline-free)
  - Busline-free variant designed for 50 MHz operation
  - Another 10 wafers in pipeline

*Busline-free design a big step!*
**In-Situ Storage Image Sensor**

- **ISIS Sensor details:**
  - CCD-like charge storage cells in each pixel, CMOS or CCD technology
  - p+ shielding implant (or epi) forms reflective barrier

- **Operational Principles:**
  - Charge collected at photogate, transferred to storage pixel during bunch train
  - 20 transfers per 1 ms bunch train
  - Readout during 200 ms quiet period after bunch train
ISIS Properties and Status

**ISIS advantages:**
- Low frequency clock -> easy to drive
- 20 kHz during capture, 1MHz readout
- \( \approx 100 \) times more radiation hard (fewer charge transfers)
- More robust to beam-induced RF pickup

**Process and Status:**
- Combines CCD and active pixel technologies
- Deep implant or custom epi needed
- Investigating CMOS and CCD vendors

*Proof of principle device (ISIS1) manufactured*
MAPS/CMOS Sensors

- p-type low-resistivity Si hosting n-type "charge collectors"
  - signal created in epi layer (low doping):
  - $Q \sim 80 \text{ e-h/}\mu\text{m} \rightarrow \text{signal} \sim 1000 \text{ e-}$
  - charge sensing through n-well/p-epi junction
  - excess carriers propagate (thermally) to diode
  - with help of reflection on boundaries
  - with p-well and substrate (high doping)

- Specific advantages of CMOS sensors:
  - Signal processing $\mu$-circuits integrated on sensor substrate (system-on-chip)
    - compact, flexible
  - Sensitive volume (~ epitaxial layer) is $\sim 10$–$15 \mu\text{m}$ thick
    - thinning to .30 $\mu\text{m}$ possible
  - Standard, massive production, fabrication technology
    - cheap, fast turn-over
  - Room temperature operation

Attractive balance between granularity, mat. budget, rad. tolerance, R/O speed and power dissipation
Monolithic Active Pixel Sensor

- Standard VLSI chip, with thin (10~15 µm) low doped epi. sensitive layer
- Intensive R&D to develop working chip since 1999:
  - MIMOSA-5 (1 Mpix, 3.5 cm²)
  - MIMOSA-20 (=M*3) (200 kpix, 1x2 cm²)
  - MIMOSA-17 (65 kpix, 0.8 x 0.8 cm²)
  - General performances well established

- new generation of full scale sensors underway : EUDET, STAR demonstrator
MAPS Status

- CMOS sensors are developed for running conditions with beam background
- Fast read-out sensors progressing steadily
  - Col-parallel architecture with discriminated output operational
  - ADCs are being developed
  - 1st generation 0-supp. μ-circuits close to fabrication
Chronopixels (CMOS)

- Buffer data during ~3000 bunches in a train and readout between bunch trains
  - bunch number stored for up to 4 samples
  - single bunch cross tagging

- 563 transistors [2 (4) buffers per pixel with calibration] into 50 x 50 µm² pixel (180 nm process)
- demonstrated performance
- ready for 80 x 80 array submission
- 20 x 20 µm² and 45 nm process
DEPFET

- Each pixel is a p-FET on a completely depleted bulk
- A deep n-implant creates a potential minimum for electrons under the gate
- ("internal gate")
- Signal electrons accumulate in the internal gate and modulate the transistor current ($g_q \sim 400 \text{ pA/e}^-$)
- Accumulated charge can be removed by a clear contact ("reset")

Fully depleted:
⇒ large signal, fast signal collection

Low capacitance, internal amplification:
⇒ low noise

Transistor on only during readout:
⇒ low power

Complete clear:
⇒ no reset noise

Compact layout:
Two pixel share common source and clear
("double pixel")
DEPFET Status

- Feasibility has been demonstrated with small devices:
  - Test beam measurements with DEPFET based telescope
  - Low intrinsic noise at ILC bandwidth
  - Radiation hardness demonstrated (Gamma, Proton & Neutron irradiations)

- Next Steps:
  - New matrix production (large, ILC scale matrices, various improvements)
  - Test new readout & control ASIC (speed, noise, radiation hardness)
  - Operate system at ILC speed

- Future Steps
  - Produce thinned matrices (2008/2009)
Properties
- Non-standard process
- Handle wafer, normally passive is the detector
- Signal collected in fully depleted substrate, thus large signals
- Electronics in the device layer
- Should be rad. hard; can have NMOS and PMOS transistors

Process Technology
- Allows for production of pixel sensors which are thin (<50 microns)
- Excellent and well controlled charge collection using fully depleted devices
- Use full CMOS readout without parasitic charge collection
- High-resistivity handle wafer as detector
EUDET: Status and Perspectives

- The EUDET initiative
- EUDET activities
  - Joint Research Activities
  - Networking
- Summary and Outlook
**EUDET**

- EUDET is an “Integrated Infrastructure Initiative (I3)” within the EU funded “6th framework programme”
- Support improvement of infrastructure for detector R&D with larger prototypes - but not the R&D itself

- EUDET is not a collaboration
  - Other institutes can contribute and exploit the infrastructure
  - Infrastructure can be re-located

### EUDET Partner Institutes

<table>
<thead>
<tr>
<th>Charles University Prague</th>
<th>INFN Ferrara</th>
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<tr>
<td>IPASCR Prague</td>
<td>INFN Milan</td>
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<td>HIP Helsinki</td>
<td>INFN Pavia</td>
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<td>INFN Rome</td>
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<td>LPC Clermont-Ferrand</td>
<td>NIKHEF Amsterdam</td>
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<td>AGH Cracow</td>
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<td>Ecole Polytechnique Palaiseau</td>
<td>CSIC Santander</td>
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<td>LAL Orsay</td>
<td>Lund University</td>
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<td>IReS Strasbourg</td>
<td>CERN Geneva</td>
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<td>CEA Saclay</td>
<td>Geneva University</td>
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<td>DESY</td>
<td>Bristol University</td>
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<td>Bonn University</td>
<td>UCL London</td>
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<td>Freiburg University</td>
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<td>MPI Munich</td>
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<td>Rostock University</td>
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<td>Tel Aviv University</td>
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</table>

+ 22 associated institutes
**EUDET Budget**

21.5 million EUR total
(7.0 million EU contribution)

- **Manpower**
  - ≈ 57 FTE total
  - ≈ 17 FTE funded by EU
    - most of the resources for the development of the infrastructures

- **Duration of 4 years**
- **Ramp-up first half 2006**
- **Full swing activities for 2.5 years**
- **Last year: phase-out and exploitation of infrastructures**
EUDET Structure

I3 projects based on three pilars:

- EUDET
  - Network
    - Management
    - Detector R&D Network
  - Transnational Access
    - Access to DESY Test Beam
  - Joint Research Activities
    - JRA1: Test Beam Infrastructures
    - JRA2: Tracking Detectors
    - JRA3: Calorimeter
Test beam Infrastructure JRA1

- Provide test beam telescope with:
  - Very high precision: <3 \( \mu \)m precision even at lower energies
  - High readout speed (frame rate >1kHz)
  - Easy to use: well defined/described interface

- Large range of conditions: cooling, positioning, magnetic field

- Suitable to different test beam environments:
  - construction & initial tests at DESY (\( E_{e^-} \) up to 6 GeV)
  - exploitation at CERN, FNAL etc. possible
JRA1 Schedule

Phase 1: “Demonstrator”
- First test facility will be available quickly for the groups developing pixels
- Use established pixel technology with analogue readout and no data reduction

Phase 2: Final telescope
- Use pixel sensor with fully digital readout, integrated Correlated Double Sampling (CDS), and data sparsification
- The beam telescope ready at the end of 2008

Detailed planning constantly being iterated

+ Large bore magnet
PCMAG Field Mapping
(Analog) Telescope

Ingredients needed for such a telescope

- Sensors with (analogue) output
- Boards to carry the sensors
- Mechanics to position the sensors precisely
- Trigger Logic Unit
- ReadOut Boards to carry the sensors
- AUX board
- EUDRB
Board Status

- 20 sets of boards
  - AUX board as interface to VME board
  - Proximity board housing the sensor (two types)

AUX board

Proximity board
Reference Plane Sensors

Demonstrator: MimoTel
- use MimoTel prototype
- AMS 0.35 OPTO process with 14 and 20μm epitaxial layer
- 4 sub-arrays (64 × 256 pixel)
  - 30 × 30 μm² pitch: active area: 7.7 × 7.7 mm²
  - readout: 1.6 ms (4 analog output nodes at 10 MHz)
  - pixel designed to stand >1 MRad at room temperature
  - engineering run was in summer 06
  - end of October, reception of engineering run

- From November to end of 2006, two tests in parallel
  - probe station setup preparation for wafer with 14 μm EPI
  - laboratory test for circuits with 20 μm EPI

Layout of the reticle of the engineering run AMS-035 OPTO 07/2006 on 14 μm (standard) and 20 μm epi substrate
MimoTel

- End of 2006 to Jan. 2007, dicing 14 µm EPI wafer
- Laboratory test for circuits with 14 µm EPI
- AMS did not respect one of our specifications: high-resistivity poly
- Biasing DACs out of range
- No effect on Mimosa18 (High Resolution Tracker)
- Small modification on the PCB board: MimoTel can be set "near" nominal conditions

General remarks:
- The dark current on rad-tol diodes (MimoTel) factor of 5 to 10 higher than expected
- The dark current on non rad-tol diodes (Mimosa18) factor of 5 to 10 lower than expected
MimoTel Results

- MimoTel (20um EPI layer)
- Response to Fe55 source at 18°C
- Noise of 15 electrons in the range of what was expected
- $K_{\beta}$ line good visible

Run 1716001; S/N seed >5

Mean value $g_1$: $331.2 \pm 0.6$
Sigma $\sigma$ $g_1$: $11.1 \pm 0.5$

Mean value $g_2$: $369.8 \pm 0.8$
Sigma $\sigma$ $g_2$: $4.1 \pm 0.6$

Mean Noise $15.4 \pm 1.6$ e
Readout: **EUDET Data Reduction Board**

**EUDRB**
- Functionality of motherboard
  - on-line calculation of pixel pedestal and noise, cluster finding, ADC
  - remote configuration of the FPGA
  - on-board diagnostics
- 4 independent signal processing and digitizing stages

**Implementation**
- One analogue card -> signal processing
- One digital card -> USB

**Operational modes**
- **Zero Suppression** readout to minimize readout dead time while normal data taking
- **Full Frame** readout mode for debugging or off-line pedestal and noise measurements

- Boards tested and available for first test in beam June 2007

**INFN Ferrara**
DAQ Integration Concept

- How to integrate the DUT hardware with the JRA1 beam telescope?
  - different groups with different detector technologies and different, pre-existing DAQ systems
  - nobody has a large pool of effort to rewrite existing code

- Use completely different hardware and DAQ for the DUT
  - synchronize only with Trigger, Busy and Reset signals
  - readout software, DAQ and data storage is provided by the DUT user
  - events combined off-line

- Trigger Logic Unit (TLU)
  - receives trigger and passes it on to telescope and DUT
  - vetoes further triggers (BUSY)
  - records timestamp
  - hardware available
**Telescope DAQ**

DAQ Software is divided into many parallel tasks:

- several **Producer** tasks read the hardware
- one **FileWriter** task bundles events, writes to file and sends subsets for monitoring
- There can be several **Online - Monitoring** tasks
- one **Buffer Monitor** task allows to see what is going on
- a **FileReader** can re-inject data into the monitoring

**Status**
- Can have several producers (Dummy, Mimosa, DEPFET, TLU) all running together.
- Data from all of them combined by FileWriter and written to binary file.
- This can then be converted to a Root file for easier analysis.
- First version will be available for test beam in June 2007
Telescope Mechanics

Box 1:
- fixed position, optical bench for three reference planes
- Wall to DUT can be removed

Box 2:
- movable in z-direction, optical bench for three reference planes
- Wall to DUT can be removed

Box 3:
- Gap between 2 and 3, closed by thermal cover
- DUT positioned on XYφ-table

XYφ-table: external with “long” mechanical structure to locate the DUT between the reference planes

boxes can be placed into magnetic field, not the XYφ-table (cost reasons)

Want to keep a lot of flexibility for different users
Senor Boxes

- Mechanics design almost completed
- 3 planes on one main structure
  - Minimal distance between planes: 7mm
  - Maximum level arm: 200 mm
- Material: aluminum
Test Beam Campaigns

- **June 2007: DESY**
  - Commissioning, First beams

- **August 2007: DESY**
  - Full system, First results

- **September 2007 (now): SPS @ CERN**
  - Demonstrate the performance:
    - Speed
    - Precision
DAQ by Geneva

Sensors etc by IRES

Mechanics/Cooling by DESY

FE Boards by INFN
DESY Test beam I

- 3 scintillator planes
- 3 sensor planes (the first two with 20 μm and the last with 14 μm epi) with one EUDRB each
DESY Test beam I

3x3 cluster signal distributions

Single track 3D hit map

First plane hit map

17 September 2007

Tobias Haas: VXD R&D
DESY Test beam II
DESY Test beam II
DESY Test beam II
Very Recent Results

# tracks/trigger

![Graph showing number of reconstructed tracks in an event with Before/after alignment and residual in X for plane 0](image)

Fiducial area of trigger scintillators

![Image of trigger scintillators and alignment](image)
Demonstrator Telescope is operational → CERN
Pixel Telescope on tour
Telescope Outlook

- The first version of the EUDET pixel telescope ("demonstrator") is now available for users.
- Full telescope with digital readout and high resolution available at the end of 2008.

You can apply for travel money through the Transnational Access and use the EUDET test beam infrastructure.

www.eudet.org

testbeam.desy.de

You can apply for test beam time at DESY (until end 2007 and after July 2008).
Conclusions

- There is a rich R&D programme for pixel sensors for a future vertex detector at an ILC.
- From the large variety of options the community will have to pick around 2 solutions around 2009/2010 to converge on a detector design.
  - Integration and DAQ issues should not be underestimated!
  - There is an R&D review initiated by the ILC management at FNAL in October.
- In the meantime projects like EUDET try to help along the way.