ASIC activities at SINTEF

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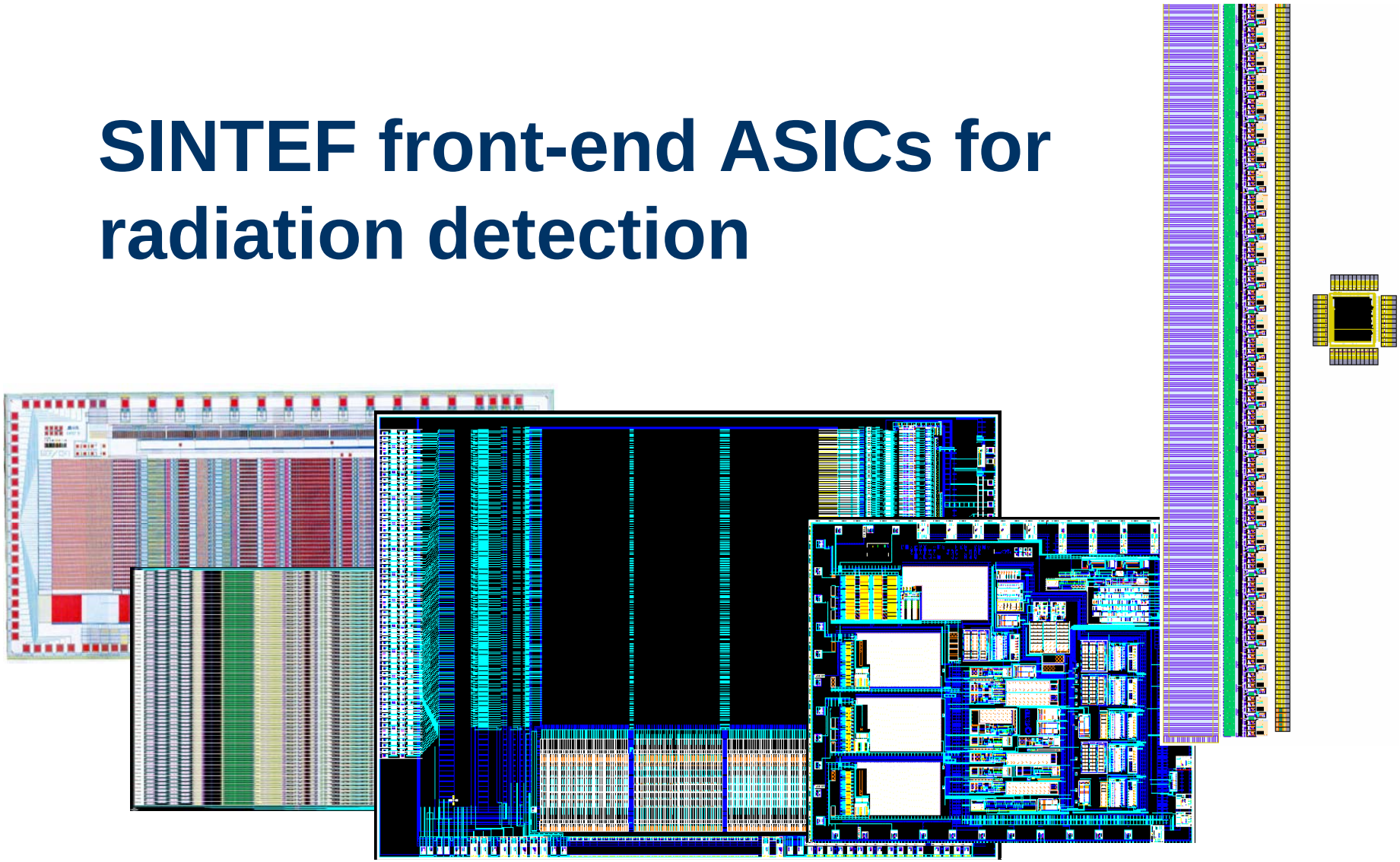
ASIC group expertise

- Analog and mixed analog/digital design
- Front-end electronics
  - High Temperature (150-250°C) CMOS and CMOS-SOI
    - Note: Similar physical phenomena occurs at hard radiation as at high temperatures. Hence also design solutions and preferred technologies are similar.
  - Biometric systems
  - RF/RFID
  - Radiation detection (light, X-ray and particles)
  - General sensor readout and front-end signal processing and management

SINTEF front-end ASICs for radiation detection

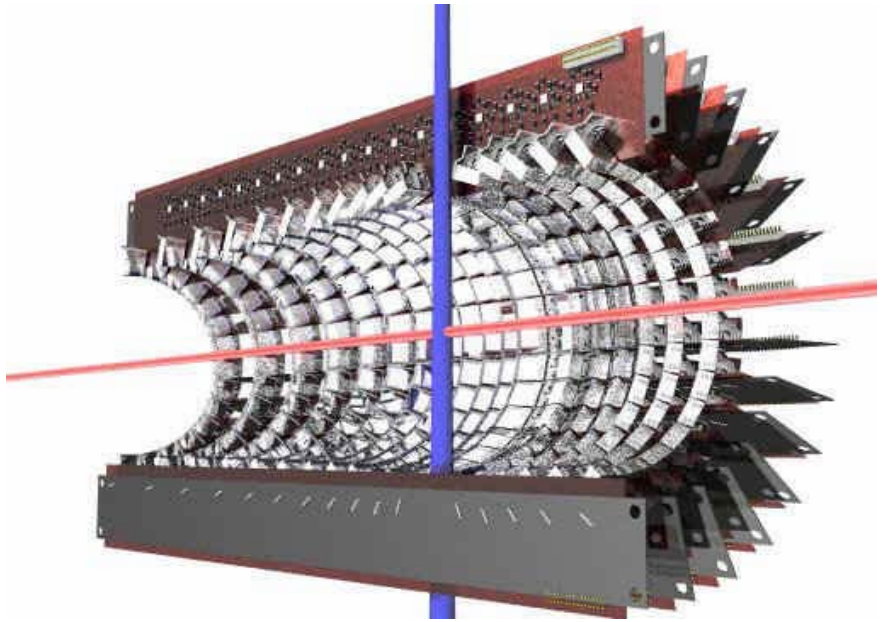


SI(NTEF) radiation expertise

- Started in 1983
- About 30-50 ASICs?
- Ideas established in 1992
- The experience of the present researchers
  - Felix — 128 channel particle detection
  - CHICsi I and II — 4 channel dE/E particle detection
  - I-ImaS — 512x32pixel X-ray (light from scintillator)
- CHICsi I (96) and CHICsi II (00)
  - Thorough tested

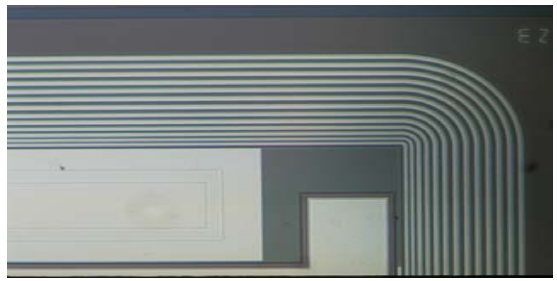
CHICsi- Celsius Heavy Ion Collaboration Si detector system

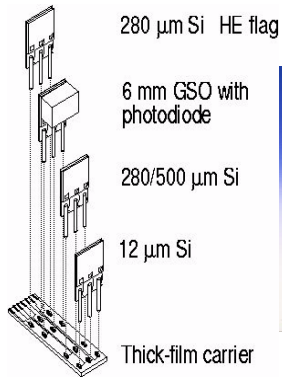
- A compact ultra-high vacuum compatible detector system for nuclear reaction experiments at storage rings
- SINTEF deliveries
  - Detectors (4000 Pcs)
  - Front-end circuits (2000 Pcs)
- Partners
  - Lund University
  - Henryk Niewodniczanski Institute of Nuclear Physics, Cracow
  - The Svedberg Laboratory, Uppsala
  - School of Technology and Society, Malmø

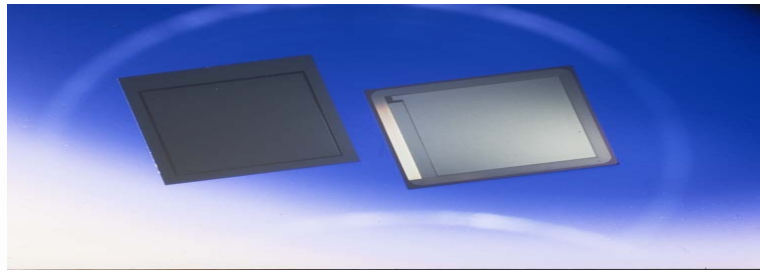


CHICSi Detector Telescopes : 12 μm Thick Silicon pin-Detectors

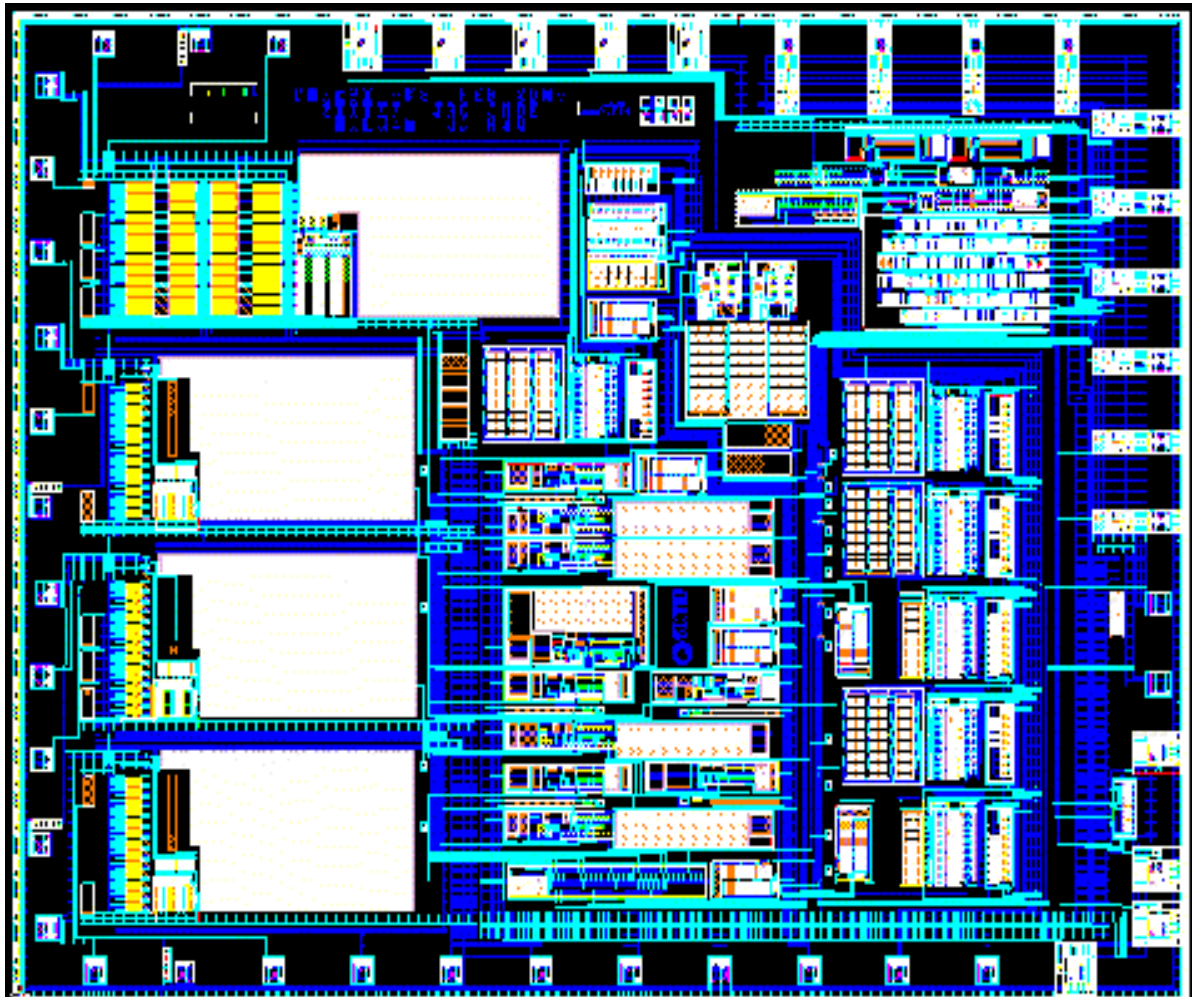
- Mass and energy measurement of light ions
- 12 μm silicon pin-diode energy loss detector
  - Active area : 1 cm^2
- Membrane fabricated by silicon etching:
  - Excellent thickness uniformity
  - Mechanical strength ➔ easy detector handling
- System: 12 μm detector + 280/500 μm detectors
- Customer:
  - CHIC collaboration
  - 1200 Pcs 12 μm
  - 2000 Pcs 280/500 μm



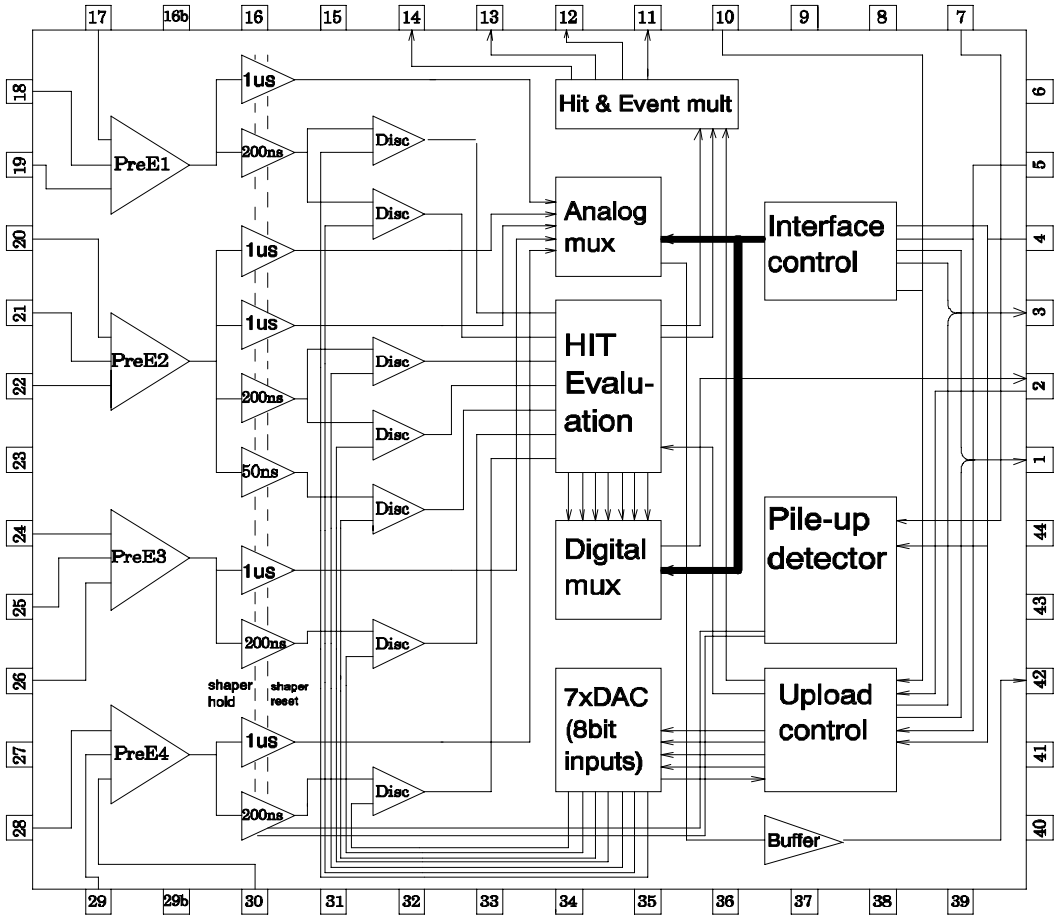




CHICsi

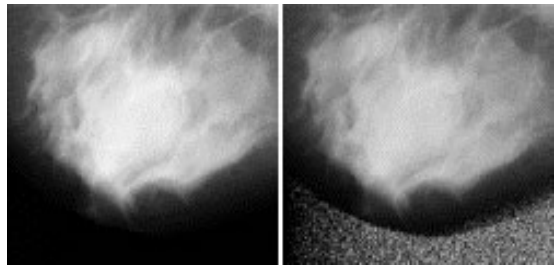


CHICsi: Block diagram

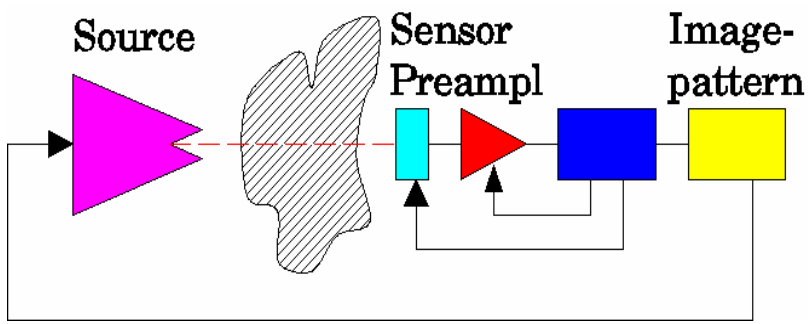


I-ImaS (Intelligent Image Sensors

- Main applications:
  - X-ray imaging for mammography and dental imaging
- Goal:
  - Improve result/cost ratio i.e. image information/x-ray dose ratio. (Same information at lower dose or more information with same dose)
- Method:
  - Optimize sensor and x-ray source parameters during picture capture.
- Require:
  - Real time processing with fast image harvest, algorithm processing, decision taking and control of electrical and mechanical parameters.
- Image size and time
  - 8 200 x 5 800 pixels read within 3 seconds



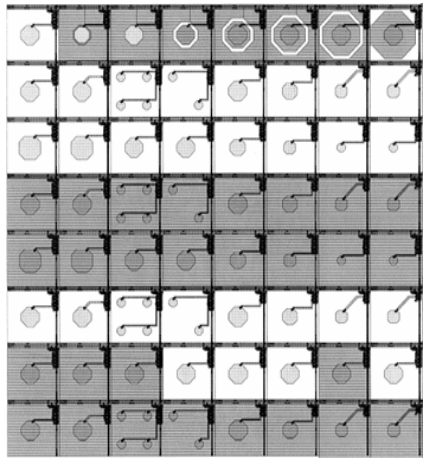
A simple algorithm reduce the beam dose by 18% without significant reduction in image information.

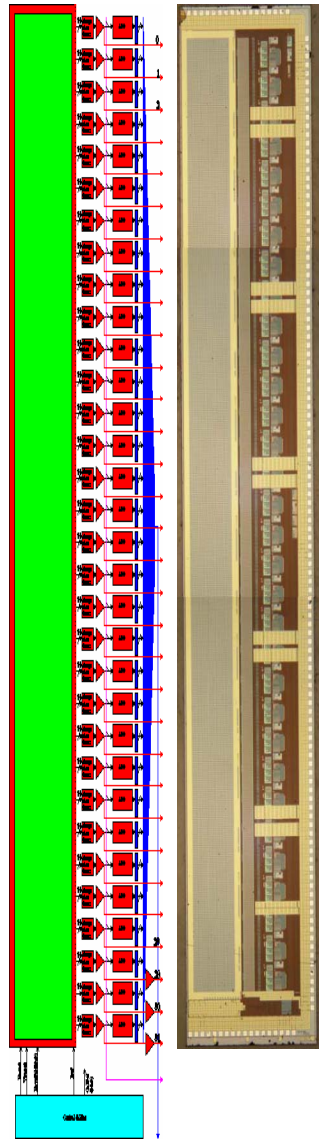


- EU founded
- Partners: UCL (UK), IC (UK), RAL (UK), ACTA (NL), UiT (IT), CTI (GR), ANCO (GR), UoI (GR), SINTEF (NO)
- SINTEF contribution: ASIC design and image processing
- Preparing for new application for the 7th frame work

SINTEF FE circuit design target

- Sensor line
  - Column of sensor ASICs scan the object
  - Scintillators on top of the sensor ASICs convert X-rays to light
- Sensor ASIC
  - Contains integrated light sensors, analogue front-end circuitry, ADCs and digital mux to external data bus
  - AMS 0.35µm Opto CMOS
  - Size 3.12mm x 17.645mm ≈ 55mm²
  - 278791 electrical elements (transistors, capacitors, etc.)
  - 148 pins
  - 40MHz clock
  - Data readout to 7-bit bus
  - Additional access points for testing
  - Additional test pixel geometries
- ASIC pixel design goal
  - 512 x 32 pixels of size 32µm x 32µm + 4 dummy pixels on all edges
  - Full well capacity: 270 000e-
  - Noise levels: 46 – 65 e- ENC
  - Fill factor: 86%
  - Several reset alternatives to reduce noise (Hard, soft and flush reset)
- ASIC analogue channels and ADCs
  - 32 analogue channels containing sampling, temporary storage and ADCs
  - On chip 10-bit SAR ADC sample in 11 periods at 1MHz. Possibility for off-chip ADCs.
  - Readout time 1-6ms





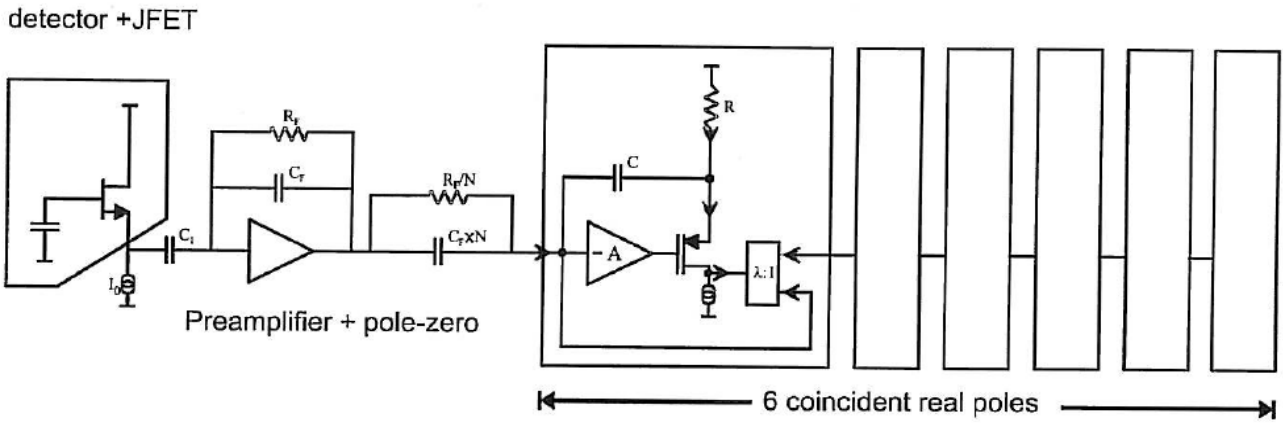
Integration of electronics and detectors

- Reasons for combining detectors and electronics on the same substrate (i.e. same wafer)
  - Noise: Amplification close to the detector strengthens the signal before it is destroyed by cross-talk/noise on connection lines
  - Capacitance: The capacitance of routing lines may be significantly larger than the optimal matching capacitance of the (small) detector capacitance
  - I/O-limitations: With increasing detector size the number of pixels grows faster than the available space for I/O along the periphery. This may put an upper limited on the possible detector size. Simple transistors used as switches can eliminate this problem.
  - Intelligence: Simple signal processing in each pixel may be used to:
    - Reduce the data output
    - Do local signal processing to optimize set up parameters on-the-fly for individual pixels or regions of pixels.

DRAGO Chip

- ”The system is based on a monolithic array of 77 silicon drift detectors (SDDs), each one with a junction field effect transistor (JFET) integrated directly on the detector chip”.
- “…aiming to achieve an electronic noise lower than 20 e-root mean square (rms) at the peaking times used for scintillation detection (e.g., 6μs to cope with the 1μs decay time of the CsI(Tl) scintillator).”
- “For low-noise solid-state detectors, like silicon drift detectors (SDDs), in X-ray spectroscopy and γ-ray imaging applications.”
- The paper focuses on the ASIC and the detector is only briefly described
  - “The circuit is composed of 8 analog channels, each including a low-noise voltage preamplifier, a 6th order semi-Gaussian shaping amplifier, with four selectable peaking times from 1.8μs up to 6μs, and a peak stretcher.”
- INFN – Istituto Nazionale di Fisica Nucleare , Milano, Italy

- Ref:
  - *DRAGO Chip: A Low-Noise CMOS Preamplifier Shaper For Silicon Detectors With Integrated Front-End JFET (2005)*
  - *An 8-Channel DRAGO Readout Circuit for Silicon Detectors With Integrated Front-End JFET (2006)*



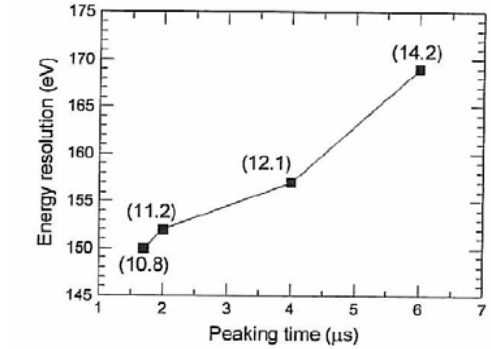


Fig. 14. Energy resolution measured at the Mn-Kα line at the four different peaking times. The corresponding value of electronics noise (in electrons rms) is reported for each measurement.

G. Zimmer, ”Technology for the compatible integration of silicon detectors with readout electronics”, *Nuclear Instruments and Methods in Physics Research 226* (1984) 175-184

- 100- high resistive substrates should be possible
- High temperatures during processing is the largest challenge: Deep wells requires higher temperatures but may reduce the carrier life time.
- Solutions:
  - N-substrate.
    - Deep p-well for isolation. N-well in p-well. Challenge: Deep p-well requires high temperature.
    - Shallow p-well around n-mos only (i.e. a twin tub). P-mos has to withstand the high bias voltages => High voltage DMOS that requires a high voltage processing step.
  - Dielectric isolation. Deep Nitrogen or Oxygen to implement an isolation silicon nitride or oxide by annealing below the transistors.

Detector	IC
Doping < 10^14cm-3 (Deep depletion layer)	Doping > 5·10^14cm-3 (Tradeoff between speed and density)
111-orientation (Simple contact technology, no edge inversion)	100-orientation (Elimination of parasitic channels in NMOS devices)
Low temperature processing (High mobility, shallow junctions)	High temperature processing (Drive in and oxidation for junction and oxide isolation)
High operation voltage (Formation of deep depletion, high carrier collection efficiency)	Low operation voltage (Compatibility to peripheral and standard electronics)
Uniform doping distribution (no distribution fields)	Shallow contact technology (Device scaling, spiking)

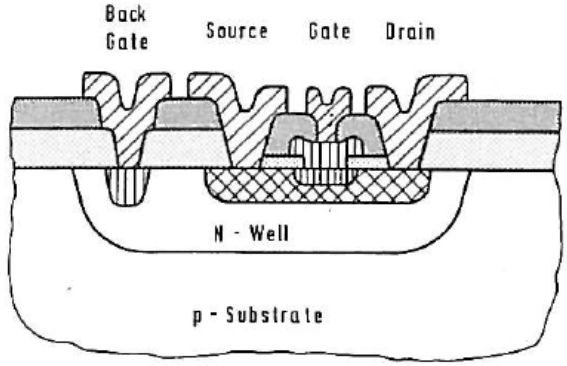


Fig. 11. Cross section of the JFET compatible with CMOS-bi-polar technology.

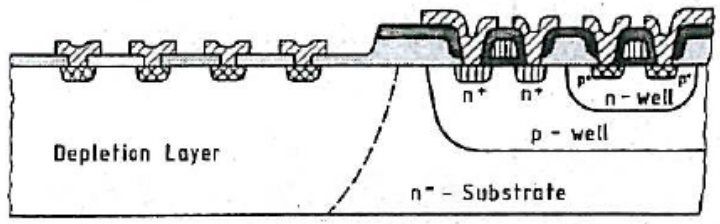


Fig. 15. Junction isolation of monolithic silicon detectors and readout electronics

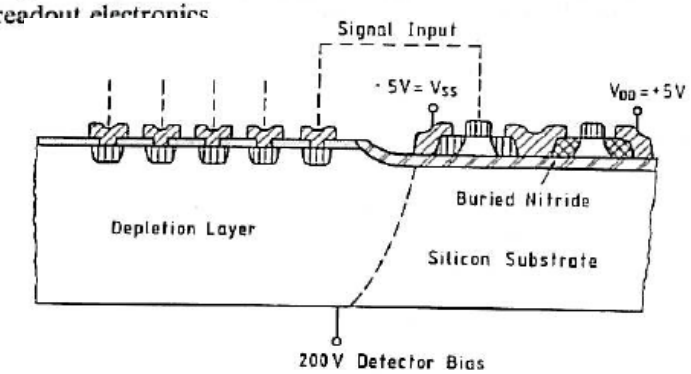


Fig. 19. Isolation scheme of silicon detector and buried nitride technology for readout electronics.

P. Rehak et.al., ”Feedback charge amplifier integrated on the detector wafer”, *Nuclear Instruments and Methods in Physics Research A288* (1990) 168-175.

- A complete charge sensitive preamplifier was realized on high resistivity detector grade silicon.
- All production steps are compatible with production steps for radiation detectors.
- Transistor elements are n-diffused Single Sided Junction Field Effect Transistor (SSJFET)
- Required implemented to match the very small anode capacitance of the detector (external stray capacitance larger than the anode capacitance). A simple source follower could not fulfil the bandwidth time requirement in time measurements.
- A 108µm wide input gate had a gate leakage current of 20pA at 293K.
- The 280µm wide input transistor had a input capacitance of 300fF.

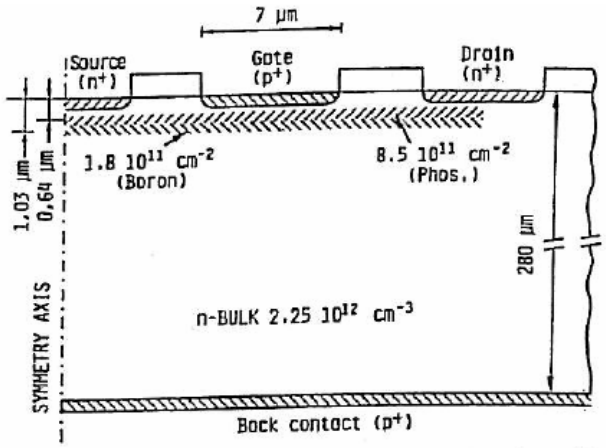


Fig. 1. Cross-section of the SSJFET. The conductive channel is obtained by a deep phosphorus implant. The substrate is high resistivity n-type silicon.

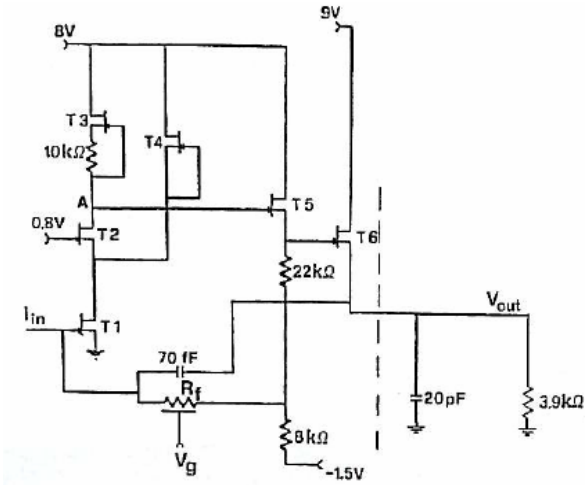


Fig. 10. Circuit diagram of the charge sensitive preamplifier.

Table 1
Parameters of the ion implants used.

	Dopant	Energy	Dose (cm^{-2})	R (µm)	s (µm)
Source, drain	P	30	5×10^{15}	0.037	0.017
Gate	B	12.5	5×10^{14}	0.033	0.017
Deep n	P	520	8.5×10^{11}	0.64	0.14
Deep p	B	480	1.8×10^{11}	1.03	0.11