DOCTORAL CANDIDATE:	Amir Hasanbegović
DEGREE:	Philosophiae Doctor
FACULTY:	The Faculty of Mathematics and Natural Sciences
DEPARTMENT:	Department of Informatics
AREA OF EXPERTISE:	Low Power, Radiation Tolerant Nanoelectronics
SUPERVISORS:	Prof. Snorre Aunet, Prof. Sunniva Siem, Prof. Oddvar Søråsen.
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DISSERTATION TITLE:	*Exploring the SEU Dependence on Supply Voltage Scaling in 90 nm and 65 nm CMOS Flip-flops*

Innovations within ultra-low power circuit design have played a key role in advancing the electronics market over the last two decades, contributing to increased portability of electronic devices, extended battery life and even self-sustained electronic systems that harvest energy from their surroundings/environment. Since space applications often have a constrained power budget, and since solar energy is often the only source of power, many space applications stand to benefit from the utilization of ultra-low power electronics and the innovations made in the terrestrial electronics market.

In this work, ultra-low power circuit design techniques are combined with radiation tolerant circuit design techniques to investigate the possibilities of realizing ultra-low power, radiation tolerant circuits for space applications. Several new and established radiation tolerant circuit topologies were implemented on prototype integrated circuits and their radiation tolerance was experimentally characterized using accelerated radiation testing.

This study shows that radiation tolerant circuits can offer lower sensitivity to radiation induced errors, compared to a standard non-radiation tolerant circuits, when scaling down the supply voltage as a means of reducing the power consumption. Simultaneously, by scaling the down supply voltage, radiation tolerant circuits can achieve up to ~12x higher energy efficiency, compared to when operating at nominal supply voltage. Supply voltage downscaling does however contribute to an increase in radiation induced errors. Nevertheless, based on the findings in this work, radiation tolerant circuits operated at reduced supply voltage offer a clear advantage over standard non-radiation tolerant circuits, and may therefore be suited for implementation in low power payloads, depending on the error rate requirements of the application.